REMARKS/ARGUMENTS

Claims 5 - 7 are pending in the application.

Claim 5 has been amended to correct the antecedence in lines 12 and 13. Claims 6 and 7 have been amended to conform their preambles to their parent claim; and claim 6 has been amended to conform an antecedence.

The rejection of claims 5, 6 and 7 under 35 U.S.C. §102(e) as being anticipated by Lin (US 6,677,668) is respectfully traversed.

Applicant's invention is directed to the problem of alleviating routing constraints on printed circuit boards and high pin counts, e.g. devices with a pin count in excess of 1000 pins (page 1, paragraph 1 of applicant's specification).

The specification then points out that current ASIC packaging uses 1 mm spacing (pitch) between pins, which allows maximum package pin counts to be in the order of 2000 pins. Pin count for future devices is expected to be higher. The specification then discusses several perspective multi-chip modules, some of which incorporate bare die, which cannot be tested at full operational speeds; and a faulty die can cause an entire module to be scrapped.

> "Consequently, the production yield of modules is related to the product of the individual yields of its component die. Hence, as the die count in a module increases its production yield decreases. This relationship has made multi-chip modules expensive to produce, and therefore they tend to be used only in cases where they are needed to meet performance requirements."
> (Specification, page 3, lines 6-12.)

The invention therefore has as its major objective the reduction of interconnection, and this is carried out in the

claims. Claim 5 calls for a tailored integrated circuit interconnect module for reducing interconnections between fully tested integrated circuit chips in which a support substrate has at least one primary integrated circuit device chip and a plurality of interacting peripheral integrated chip devices thereon.

> "...said interconnect module including a plurality of interface pins, each integrated circuit device having a plurality of interface ports, at least one of which is connected to another one of said plurality of integrated circuit devices."

At least one of the integrated circuit devices has an interface port connected to an interface pin whereby the nodes on the peripheral devices are adapted to interface with nodes of at least one primary integrated chip device in such a way as to condense the number of nets so that the total number of nodes connected to external pins may be minimized. There is nothing in the Lin disclosure which suggests, teaches, hints or has any relation to reducing or condensing the number of nets so that the total number of nodes connected to external pins may be minimized. There is no teaching or suggestion in Lin of each integrated circuit device having a plurality of interface ports, at least one of which is connected to another one of the plurality of integrated circuit devices. As set out on page 9 of applicant's specification, the main advantages of his invention are that it enables circuit boards to be routed using fewer board layers; and, unlike prior art multi-chip modules, the tailored interconnect module of this invention integrates fully tested devices in chip scale packages in a single

package, thereby trading-off intra-device performance for an improvement in manufacturing yield.

It is interesting to note that none of the terms of applicant's claims "pin," "port," "interface," "interconnection," "interconnect," and "nodes" is disclosed or used in applicant's sense in the Lin disclosure. While the Examiner has correctly equated the term "pin" to solder balls, solder columns and other, there is no equating applicant's port, interface, interconnection, interconnect, or nodes to equivalent terms of the reference. Clearly, the Examiner has given meaning of these terms in light of the reference which is unwarranted.

In view of the above, further and favorable reconsideration is respectfully requested.

Respectfully submitted,

Jim Zegeer, Reg. No. 18,957
Attorney for Applicant

Suite 108
801 North Pitt Street
Alexandria, VA 22314
Telephone: 703-684-8333

Date: January 12, 2005